Annexure A

M.Tech in Electronics and Communication Engineering
Specialization: Microelectronics and VLSI Design

FIRST YEAR

FIRST SEMESTER

A. Theory							
Sl. No	**Code**	**Paper**	**Contact Periods/Week**				**Credits**
			L	T	P	Total	
1.	MECE-101	Semiconductor Device Physics	4	1	--	5	5
2.	MECE-102	Digital VLSI Design	4	1	--	5	5
3.	MECE-103	Microelectronics Technology	4	1	--	5	5
4.	MECE-104	Digital Signal Processing	4	1	--	5	5
5.	MECE-105	Hardware Description Language	4	0	--	4	4
Total Theory			20	4	--	**24**	**24**
B. Practical							
1.	MECE-106	Front End VLSI Design Lab	--	--	6	6	3
2.	MECE-107	Back End VLSI Design Lab	--	--	6	6	3
3.	MECE-108	Grand Viva I*	--	--	--	--	5
Total Practical					12	**12**	**11**
Total of Semester:						**36**	**35**

SECOND SEMESTER

A. Theory							
Sl. No	**Code**	**Paper**	**Contact Periods/Week**				**Credits**
			L	T	P	Total	
1.	MECE-201	Analog VLSI Design	4	1	--	5	4
2.	MECE-202	VLSI Physical Design	4	1	--	5	4
3.	MECE-203	Verification and Testing	4	1	--	5	4
4.	MECE-204	Elective – I	4	1	--	5	4
5.	MECE-205	Elective – II	4	0	--	4	3
Total Theory			20	4	--	**24**	**24**
B. Practical			L	T	P		
1	MECE-206	Advanced Analog VLSI Design Lab	--	--	6	6	3
2	MECE-207	Advanced Digital VLSI Design Lab	--	--	6	6	3
3	MECE-208	Grand Viva II*	--	--	--	--	5
Total Practical			--	--		**12**	**11**
Total of Semester:						**36**	**35**

*** Based on semester subjects.**

Elective – I	**Elective – II**
A. Timing Analysis	A. Biomedical Signal Processing
B. Quantum and Nanoelectronics	B. Low Power VLSI Design
C. Advanced Digital Architecture	C. Embedded System Design
D. CAD for VLSI Design	D. RF Integrated Circuits
E. MEMS and NEMS Technology	E. Image Processing

SECOND YEAR

THIRD SEMESTER

A. Theory							
Sl. No.	**Code**	**Paper**	**Contact Periods/Week**				**Credits**
			L	T	P	Total	
1	MECE-301	Project I	--	--	--	--	15
2	MECE-302	Term Paper on Project	--	--	--	--	10
Total of Semester:							**25**

FOURTH SEMESTER

A. Theory							
Sl. No.	**Code**	**Paper**	**Contact Periods/Week**				**Credits**
			L	T	P	Total	
1	MECE-401	Project II	--	--	--	--	25
Total of Semester:							**25**

Paper Code: MECE-101
Paper Name: Semiconductor Device Physics

Unit I: Crystal and Electronic Band Structure of Semiconductor

Crystal structure- Reciprocal lattice -Brillouin zone and rules for band (*k* - space) representation, Dynamics of electrons in periodic potential: Kronig -penny and nearly free electron models – Real methods for band structure calculations, Energy band diagrams of III-V semiconductors and metal-semiconductor interface, Block wave functions, concepts of effective mass, Density of states, wave vector, Direct and Indirect semiconductor, quantisation of vibrational energy, phonons, defect dislocation and impurity states.

Unit II: Carries in Semiconductor Devices

Free carrier in semiconductor, statistical distribution, Fermi energy in degenerate and non-degenerate semiconductors, of quasi-Fermi levels, Transport phenomena in Semiconductor – Bolzman transport equation, scattering mechanisms, mobility diffusion, physics of High-electron-mobility transistor. Ballistic transport mechanism, Macroscopic transport: Carrier transport by Diffusion – Continuity and Poisson equation, Carrier transport by Drift and diffusion: Low field, High field and very high field (Impact ionization) – Einstein relation. Hall-effect and voltage, P-n Junctions: equilibrium conditions, forward and reverse-biased junctions, reverse-bias breakdown, transient and a-c conditions, recombination and generation in the transition, semiconductor heterojunctions, Metal-semiconductor junctions: Schottky barriers, rectifying and Ohmic contacts.

Unit III: Transistor Device Physics

Bipolar junction transistors: minority carrier distribution and terminal currents, generalized biasing, switching, secondary effects, frequency limitations of transistors, early effect, punch-through, ebers-moll model of BJT, heterojunction bipolar transistors, Field-Effect Transistors: JFET- current-voltage characteristics, effects in real devices, high-frequency and high-speed issues, Metal Insulator Semiconductor FET, MOSFET- basic operation and fabrication; ideal MOS capacitor; effects of real surfaces; threshold voltages; output and transfer characteristics of MOSFET, short channel and Narrow width effects: Drain Induced barrier lowering (DIBL), Gate-Induced drain leakage (GIDL), hot carrier degradation, velocity saturation, MOSFET scaling, Physics of FinFET, Juntion less Transistor, SPICE Models for Semiconductor Devices.

Unit IV: Physics of Optoelectronic Devices

Optoelectronics Devices: Light emitting diodes, Lasers, Photoconductors, Junction Photodiodes, Avalanche Photodiodes, Solar Cells, Semiconductor based microwave devices: Tunnel diode, Gunn diode, IMPATT diode, TRAPATT diode, PIN diode, varactor diode

Unit V: Physics of Power Electronic Devices

High Power semiconductor device: Power diode, Power MOSFET, Thyristors: Gate Turn-Off thyristor (GTO), Silicon Controlled Rectifier (SCR), TRIAC, DIAC.

Text Books:

1. Kevin F Brennan, "The Physics of Semiconductors", Cambridge Univ. Press, 1999.
2. S. A. Neamen and D. Biswas, Semiconductor Physics and Devices, 4th Edition, TMH, 2012.

Reference Books:

1. S. M. Sze and K. K. Ng, "Physics of Semiconductor Devices", 3rd Edition, Wiley India, 2010.
1. Kittel Charles, "Introduction to Solid State Physics", 6th Ed., Willey (1991).
2. P. Bhattacharya, Semiconductor Optoelectronics Devices, 2nd Edition, PHI, 2009.
3. Streetman, B.G. and Banerjee, S.K, "Solid State Electronic Devices", 7th Ed., Pearson Education, 2016.

Paper Code: MECE-102
Paper Name: Digital VLSI Design

Unit – 1
Review of MOSFET characteristics, Scaling and small-geometry effects, MOSFET capacitances, MOS Inverter, CMOS Inverters. Introduction MOSFET, threshold voltage, current, Channel length modulation, body bias effect and short channel effects, MOS switch, MOSFET capacitances, MOSFET models for calculation-Transistors and Layout, CMOS layout elements, parasitics, wires and vias-design rules-layout design SPICE simulation of MOSFET I-V characteristics and parameter extraction

Unit – 2
Combinational MOS Logic Circuits (including CMOS logic domino logic, Pseudo-NMOS), CMOS inverter, static characteristics, noise margin, effect of process variation, supply scaling, dynamic characteristics, inverter design for a given VTC and speed, effect of input rise time and fall time, static and dynamic power dissipation, energy & power delay product, sizing chain of inverters, latch up effect-Simulation of static and dynamic characteristics, layout, post layout simulation

Unit – 3
Sequential MOS Logic Circuits, Dynamic Logic Circuits, Static CMOS design, Complementary CMOS, static properties, propagation delay, Elmore delay model, power consumption, low power design techniques, logical effort for transistor sizing, ratioed logic, pseudo NMOS inverter, DCVSL, PTL, DPTL & Transmission gate logic, dynamic CMOS design, speed and power considerations, Domino logic and its derivatives, C2MOS, TSPC registers, NORA CMOS –Course project

Unit – 4
Low-Power CMOS Logic Circuits, BiCMOS Logic Circuits, Circuit design considerations of Arithmetic circuits, shifter, CMOS memory design – SRAM and DRAM, BiCMOS logic - static and dynamic behaviour -Delay and power consumption in BiCMOS Logic

Unit – 5
FPGA logic element and interconnect architecture, Logic synthesis for FPGA ,Physical design for FPGA, Input-Output Circuits, ESD protection circuit.

Text Books:
1. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis &Design, , MGH, Third Ed., 2003
2. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective,Prentice Hall, SecondEdition, 2005.
Reference Books:
3. David A. Hodges, Horace G. Jackson, and Resve A. Saleh, Analysis and Design of DigitalIntegrated Circuits, Third Edition, McGraw-Hill, 2004
4. R. J. Baker, H. W. Li, and D. E. Boyce, CMOS circuit design, layout, and simulation,Wiley-IEEE Press, 2007
5. Christopher Saint and Judy Saint, IC layout basics: A practical guide, McGraw-Hill6Professional, 2001

Paper Code: MECE-103
Paper Name: Microelectronics Technology

Unit I: Crystal Growth, Epitaxy, Oxidation

Clean room concept – Growth of single crystal Si, Crystal growth using Czochralski's method, Float Zone method and Bridgeman technique, Zone refining, characteristics and crystal evaluation, Surface contamination, Defects in Crystal, cleaning & etching, Cleaning of p-type & n-type Si-wafer by solvent method & RCA cleaning, Wafer Shaping operations, Slicing, polishing and etching, Importance of epitaxial layer growth, Types of epitaxy: VPE, MBE, MOCVD Defects in epitaxial layers and their removal, Oxidation Techniques and Systems, Kinetics of Oxidation, Oxide properties, Redistribution of Dopant At interface, Oxidation of Poly Silicon, Oxidation inducted Defects.

Unit II: Lithography, Etching, Deposition

Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, Etching, Dry Etching, Reactive Plasma Etching techniques and Equipments, Wet Chemical Plasma deposition, Thin film and Thick film technology: Processing techniques, applications and advantages, Thin film deposition techniques: Epitaxy, VDE, CVD, PECVD, PVD, Sputtering ,MBE and epitaxial layer evaluations, Patterning.

Unit III: Diffusion, Ion Implantation, IC fabrication

Solid State Diffusion – Fick's equation, atomic diffusion mechanisms, measurement techniques, diffusion in polysilicon and silicon dioxide diffusion systems, Ion implantation – Range theory, Equipments, annealing, shallow junction, high energy implementation, Monolithic IC Technologies: Diodes, Resistors, Capacitors, Transistors: FETs, Polysilicon gates and Well Structures, NMOS, CMOS, MOS Memory, Bipolar ICs, IC crossover, Process Monitoring.

Unit IV: Metallization, MEMS Fabrication

Metallization and Interconnects. Introduction to MEMS fabrication Technologies. Future trends and Challenges: Challenges for integration, system on chip.

Unit V: Packaging

Packaging design considerations, Reliability, Testability, Package Types, IC bonding and Encapsulation, Mountings in packages using Dual-in-line (DIP) or TO packages, Packages using surface-mount-technology (SMT)

Text Books:

3. S. M. Sze, "VLSI Technology," 2nd Ed., TMH, 2008.
4. S.K. Gandhi, "VLSI Fabrication Principles: Silicon and Gallium Arsenide," 2nd Ed, Wiley, 2008.

Reference Books:

2. J. D. Plummer, M. D. Deal and P. B. Griffin, "Silicon VLSI Technology, Fundamentals, Practice and Modeling," Pearson education, 2000.
3. G. S. May and S. M. Sze, "Fundamentals of Semiconductor Fabrication," Wiley India, 2004.
4. M. J. Madou, "Fundamentals of Microfabrication," 2nd Ed., CRC Press, 2011.
5. Mohamed Gad-el-Hak, "MEMS: Design and Fabrication," 2nd Ed., CRC Press, 2005.

Paper Code: MECE-104
Paper Name: Digital Signal Processing

Unit I:
Review of discrete time signals, systems and transforms: Discrete time signals, systems and their classification, analysis of discrete time LTI systems: impulse response, difference equation, frequency response, Transfer function, DTFT, DTFS and Z-transform.

Unit II:
Discrete Fourier Transform (DFT): Computational problem, DFT relations, DFT properties, fast Fourier transform (FFT) algorithms (radix-2, decimation-in-time, decimation-in-frequency), Goertzel algorithm, linear and circular convolution using DFT.

Unit III:
Filters design and their characteristics: Frequency selective filters: Ideal filter Characteristics, lowpass, highpass, bandpass and bandstop filters, notch filters, all-pass filters, Structures for discrete-time systems: Signal flow graph representation, basic structures for FIR and IIR systems (direct, parallel, cascade and polyphase forms), transposition theorem, ladder and lattice structures.

Unit IV:
Design of FIR and IIR filters: Design of FIR filters using windows, frequency sampling, Design of IIR filters using impulse invariance, bilinear transformation and frequency transformations.

Unit V:
Finite word length effects in digital filters: Fixed and floating point representation of numbers, quantization noise in signal representations, finite wordlength effects in coefficient representation, roundoff noise, SQNR computation and limit cycle. Introduction to multirate signal processing: Decimation, interpolation, polyphase decomposition; digital filter banks: Nyquist filters, two channel quadrature mirror filter bank and perfect reconstruction filter banks, subband coding.

Text Books:

1. Digital Signal Processing – Principles, Algorithms and Applications by J. G. Proakis and D. G. Manolakis, Pearson. Latest Edition.
2. Digital signal Processing by Salivahanan, TMH, Latest Edition.

Reference Books:

1. Johnny R. Johnson, Introduction to Digital Signal Processing..A. V. Oppenheim and R.W. Schafer, Digital Signal Processing, PHI Latest Edition.
2. A.V. Oppenheim and R.W. Schafer, Digital Signal Processing. Latest Edition.
3. Sanjit and Mitra, Digital Signal Processing, Tata McGraw Hill. Latest Edition.
4. A.V. Oppenheim and R.W. Schafer, Discrete Time Signal Processing, Pearson Education Ltd. Latest Edition.

Paper Code: MECE-105
Paper Name: Hardware Description Language

UNIT-I:

INTRODUCTION TO VHDL: VHDL description, combinational, networks, modeling flip flop using VHDL, VHDL model for multiplexer, compliance and simulation of VHDL, codes, modeling a sequential machine, variables, signals and constants, arrays VHDL operators, VHDL functions, VHDL procedures, packages and libraries, VHDL model for a counter.

ADVANCED VHDL: Attributes, transport and inertial delays, operator over loading, multi valued logic and signal resolution, IEEE-1164, standard logic, generic, generates statements, synthesis of VHDL codes, synthesis examples, file handling and TEXTIO.

UNIT-II:

DESIGN OF NETWORKS FOR ARITHMATIC OPERATIONS: Design of serial adder with accumulator, state graph for control networks design of binary multiplier, multiplication of signed binary numbers design of binary divider.
DIGITAL DESIGN WITH SM CHART: state machine charts, derivation of SM charts, realization of SM charts, implementation of dice game, alternative realization of SM charts using microprogramming, linked state machine.

UNIT-III:

FLOATING POINT ARITHMETIC: Representation of floating point numbers, floating point multiplication and other floating point operations.
DESIGNING WITH PROGRAMMABLE GATE ARRAYS AND COMPLEX
PROGRAMMABLE LOGIC DEVICES: Xinx 3000 series FPGAs, Xinx 4000 series FPGAs, using one hot state assignment.

UNIT-IV:

MEMORY MODELS FOR MEMORIES AND BUSES: Static RAM, a simplified 486 bus model, interfacing memory to microprocessor bus.

UNIT-V:

DESIGN EXAMPLES: UART design, description of MC68HC05 microcontroller, and design of micro-controller CPU, complete microcontroller design.

TEXT BOOKS:

1. J. Bhaskar, " A VHDL Primer", Addison Wesley, 1999.
2. C. H. Roth, "Digital System Design using VHDL", PWS Publishing, 2003.

REFERENCES BOOKS:

1. M. Ercegovac, T. Lang and L.J. Moreno, "Introduction to Digital Systems", Wiley,2000
2. J.F. Wakerly, "Digital Design-Principles and Practices", PHL, 2000.
3. Douglas Perry, "VHDL", MGH, 2000.
4. Michae John Sebastian Smith, "Application-Specific Integrated Circuits", Addison-Wesley, 2000.
5. Z. Navabi, " VHDL-Analysis and Modeling of Digital Systems", MGH, 2000.
6. Peter J. Ashenden, Designers guide to VHDL, , Morgan Kaufman Publishers.

Paper Code: MECE-106
Paper Name: Front End VLSI Design Lab

Modeling and Functional Simulation of the following digital circuits (with Xilinx/ ModelSim /Cadence tools) using VHDL/Verilog Hardware Description Languages

1. Basic Logic Gates.
2. Multiplexer, Comparator, Adder/ Substractor, Multipliers, Decoders.
3. D-Latch, D-Flip Flop, JK-Flip Flop, Registers.
4. Combinational Logic: Address decoders, parity generator, ALU
5. Sequential Logic: Ripple Counters, Synchronous Counters, Shift Registers (serial-to-parallel, parallel-to-serial), Cyclic Encoder / Decoder.

Paper Code: MECE-107
Paper Name: Back End VLSI Design Lab

Session –I: Digital IC Design Laboratory

1. Introduction to SPICE (operating point Analysis, DC Sweep, Transient Analysis, Transfer Function Analysis)

2. An Overview of Cadence Environment/Tanner EDA Tool/Electric/Magic/ NG spice/LTspice.

3. I-V Curve of NMOS & PMOS Transistor (Parametric Analysis)

4. DC analysis of CMOS Inverter(VTC, Noise Margin), Dynamic Characteristics of CMOS Inverters(Propagation Delay , Power Dissipation).

5. Schematic Entry /Simulation/Layout of CMOS Combinational & Sequential Circuits.(Also Design High Speed and Low power)

Session –II: Analog IC Design Laboratory

1. Design & Simulation and also analysis of frequency response of various amplifier s (Single Stage, Differential amplifier),Basic Current Mirror, Cascode Current mirror.

2. Introduction to basic layouts
   a. Layout of an inverter
   b. Layout of standard cells : what to takes care of (pitch, reduction of area)
   c. Layout of a level shifter: introduction to deep-n well process. How to take care of LVS with different grounds in a non-deep-n well process using pseudo PSUB layers.
   d. Layout of a basic current mirror: introduction to matching and dummies.
   e. Layout of a differential amplifier: introduction to power-planning, floor plan and understanding the signal flow path.

Paper Code: MECE-108
Paper Name: Grand Viva I

Based on semester subjects

Paper Code: MECE-201
Paper Name: Analog VLSI Design

Unit – 1
Introduction to Analog Design, Basic MOS Device Physics: MOSFET as a switch, MOS I/V characteristics and MOS Device model.

Unit – 2
Amplifiers: Analysis of Single stage and Differential amplifiers. Passive and Active Mirrors, Frequency Response of Amplifiers, Noise: Statistical Characteristic of Noise, Type of Noise, and Noise in Single stage amplifiers.

Unit – 3
Feedback topologies, Effect of Loading, Operational Amplifiers, Stability and Frequency Compensation, Bandgap References, Introduction to switched Capacitor Circuits, Nonlinearity and Mismatch, Oscillators,

Unit – 4
Short-channel Effects and Device Models: Scaling theory, Threshold Voltage Variation, Mobility Degradation with Vertical field, Velocity Saturation, Hot Carrier effect, MOS device Models: Level 1model, level 2 model, level 3 model, charge and Capacitance Modeling, Temperature dependence.

Unit - 5
Basic MOS device & model, Basic CMOS device, MOS resistor, MOS current source, current Sink, Current Mirror circuits, operational amplifier design (OPAMP), differential amplifier, level shifter, Source follower, Compensation techniques, BiCMOS device and technology, pass transistor logic. Analog Filter: Switched capacitor (SC) fundamentals, first order and second order SC circuits. VLSI interconnects: Physics of interconnects in VLSI, distributed RC model, Future interconnect technology.

Text Books:

1. Behzad Razavi, Design of Analog CMOS Integrated Circuit, Tata-Mc Graw Hill, 2002.

References:

1. David A Johns & Ken Martin, Analog Integrated Circuit Design, John Wiley and Sons, 2001.
2. 3. Philip Allen & Douglas Holberg, CMOS Analog Circuit Design, Oxford University Press, 2002.

Paper Code: MECE-202
Paper Name: VLSI Physical Design

Unit -I

VLSI Physical Design Automation: VLSI Design Cycle, Physical Design Cycle, Design Styles, System Packaging Styles, Historical Perspectives.

Unit-II

Existing Design Tools Design and Fabrication of VLSI Devices: Fabrication Materials, Transistor Fundamentals, Fabrication of VLSI Circuits, Design Rules.

Unit-III

Layout of Basic Devices Fabrication Process and its Impact on Physical Design: Scaling Methods, Status of Fabrication Process, Issues Related to the Fabrication Process, Future of Fabrication Process, Solutions for Interconnect Issues, Tools for Process Development

Unit – IV

Data Structure and Basic Algorithms: Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, Graph Algorithm for Physical Design Partitioning: Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithm, Simulated Annealing and Evolution, Other Partitioning Algorithms, Performance Driven Partitioning Floor Planning and Pin assignment: Floor Planning, Chip Planning, Pin Assignment, Integrated Approach

Unit -V

Placement: Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Performance Driven Placement Over-the-Cell Routing and Via Minimisation, Clock and Power Routing: Over-the-Cell Routing, Via Minimisation, Clock Routing, Power and Ground Routing Physical Design Automation of FPGAs: FPGA Technologies, Physical Design Cycle for FPGAs, Partitioning, Routing Physical Design Automation of MCMs: MCM Technologies, MCM Physical Design Cycle, Partitioning, Placement, Routing

Text Books:

1. Naved A. Sherwani, Algorithms for VLSI Physical Design Automation, 3rd Edn., Springer (India) Pvt. Ltd., 2005, ISBN: 0792383931

Reference Books:

1. Gerez, Algorithms for VLSI Design Automation, Wiley India Pvt. Ltd., New Delhi, ISBN 10: – 8126508211, ISBN 13: – 9788126508211.

Paper Code: MECE-203
Paper Name: Verification and Testing

Unit 1

Scope of testing and verification in VLSI design process, Issues in test and verification of complex chips, embedded cores and SOCs.

Unit 2

Fundamentals of VLSI testing Fault models. Automatic test pattern generation, Design for testability, Scan design, Test interface and boundary scan. System testing and test for SOCs. Delay fault testing.

Unit 3

BIST for testing of logic and memories, Test automation, Design verification techniques based on simulation, analytical and formal approaches.

Unit 4

Functional verification, Timing verification, Formal verification, Basics of equivalence checking and model checking, Hardware emulation.

Unit 5

Test generation for combinational circuits –D-algorithm etc. Test pattern generation for sequential circuits-boundary scan(JTAG) Built in self-test techniques Non-intrusive automated testing Functional testing

Text Books:

1. M. Bushnell and V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Kluwer Academic Publishers, 2000.
2. M. Abramovici, M. A. Breuer and A. D. Friedman, Digital Systems Testing and Testable Design, IEEE Press, 1990. 3. T.Kropf, Introduction to Formal Hardware Verification, Springer Verlag, 2000.

References:

3.P. Rashinkar, Paterson and L. Singh, System-on-a-Chip Verification Methodology and Techniques, Kluwer Academic Publishers, 2001.
4. Neil H. E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Second Edition, Addison Wesley, 1993.

6. Neil H. E. Weste and David Harris, Principles of CMOS VLSI Design, Third Edition, Addison Wesley, 2004.

Paper Code : MECE-204
Paper Name: Elective – I

A. Timing Analysis
B. Quantum and Nanoelectronics
C. Advanced Digital Architecture
D. CAD for VLSI Design
E. MEMS and NEMS Technology

A. Timing Analysis

Unit 1

Introduction to timing path and arrival time, Introduction to required time and slack, Introduction to basic categories of setup and hold analysis, Introduction to data check and latch timing, Introduction to slew, load and clock checks

Unit 2

Convert logic gates into nodes, Compute actual arrival time (AAT), Compute required arrival time (RAT), Compute slack and introduction to GBA-PBA analysis, Convert pins to nodes and compute AAT, RAT and slack

Unit 3

Introduction to transistor level circuit for flops, Negative and positive latch transistor level operation, Library setup time calculation, Clk-q delay calculation, Steps to create eye diagram for jitter analysis, Jitter extraction and accounting in setup timing analysis

Unit 4

Setup analysis - graphical to textual representation, Hold analysis with real clocks, Hold analysis - graphical to textual representation, crosstalk

Unit 5

On chip variation (OCV), Sources of variation – etching, Sources of variation - oxide thickness, Relationship between resistance, drain current and delay, OCV based setup timing analysis, Setup timing analysis after pessimism removal, OCV based hold timing analysis, Hold timing analysis after pessimism removal.

Text Books:

1. Michae John Sebastian Smith, "Application-Specific Integrated Circuits", Addison-Wesley, 2000

Reference Books:

2. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis &Design, , MGH, Third Ed., 2003
3. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective,Prentice Hall, SecondEdition, 2005.

B. Quantum and Nanoelectronics

Unit 1

Challenges going to sub-100 nm MOSFETs – Oxide layer thickness, tunneling, power density, non-uniform dopant concentration, threshold voltage scaling, lithography, hot electron effects, sub-threshold current, velocity saturation, interconnect issues, fundamental limits for MOS operation. High-K gate dielectrics, effects of high-K gate dielectrics on MOSFET performance,

Unit 2

Novel MOS-based devices – Multiple gate MOSFETs, Silicon-on-nothing, Silicon-on-insulator devices, FD SOI, PD SOI, FinFETs, vertical MOSFETs, strained Si devices

Unit 3

Hetero structure based devices – Type I, II and III Heterojunction, Si-Ge heterostructure, hetero structures of III-V and II-VI compounds - resonant tunneling devices, MODFET/HEMT

Unit 4

Carbon nanotubes based devices – CNFET, characteristics, Spin-based devices – spinFET, characteristics

Unit 5

Quantum structures – quantum wells, quantum wires and quantum dots, Single electron devices – charge quantization, energy quantization, Coulomb blockade, Coulomb staircase, Bloch oscillations

Text Books:

1. Mircea Dragoman and Daniela Dragoman, Nanoelectronics – Principles & devices, Artech House Publishers, 2005.

2. Karl Goser, Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices, Springer 2005.

3. Mark Lundstrom and Jing Guo, Nanoscale Transistors: Device Physics, Modeling and Simulation, Springer, 2005.

References:

4. Vladimir V Mitin, Viatcheslav A Kochelap and Michael A Stroscio, Quantum heterostructures, Cambridge University Press, 1999.

5. S.M. Sze (Ed), High speed semiconductor devices, Wiley, 1990. 6. Manijeh Razeghi, Technology of Quantum Devices, Springer, ISBN 978-1-4419-1055-4.

7. H.R. Huff and D.C. Gilmer, High Dielectric Constant Materials for VLSI MOSFET Applications, Springer 2005, ISBN 978-3-540-21081-8 , (Available on NITC intranet in Springer eBook section)

8.B.R. Nag, Physics of Quantum Well Devices, Springer 2002, ISBN 978-0-7923-6576-1, (Available on NITC intranet in Springer eBook section).

9. E.Kasper, D.J. Paul, Silicon Quantum Integrated Circuits Silicon-Germanium Heterostructures Devices: Basics and Realisations, Springer 2005, ISBN 978-3-540-22050-3, (Available on NITC intranet in Springer eBook section).

C. Advanced Digital Architecture

Unit 1:Combinational Logic Design:

Concept of hierarchical design, technology mapping, decoder & decoder based combinational circuit design, encoder & priority encoder, multiplexer & multiplexer based combinational circuit design, binary adders, binary subtractor, adder-subtractor, other arithmetic functions: contraction, increment/decrement, constant multiplication/division, zero filling, extension.

Unit 2:Sequential Circuits:

Basics of sequential circuits, latches, flip-flops, sequential circuit analysis, state equation, state diagram, state table, sequential circuit design, state assignment, state encoding, state machine diagram, design applications. Flip-flop timing, sequential circuit timing analysis.Concept of asynchronous & synchronous circuits.

Unit 3:Programmable Logic Design, Register, Counter:

Read only memory, programmable logic array, programmable array logic, field programmable array logic, registers: serial-in-parallel out, serial-in-serial-out, parallel-in-serial-out, parallel-in-parallel-out, register transfer operations. Micro-operations, arithmetic, logic, shift, arithmetic & logic shift, barrel shifter, counters.

Unit 4:Memory:

Basic definitions, random-access memory, SRAM integrated circuit, SRAM array, DRAM integrated circuit, DRAM types, DRAM array, CAM.

Unit 5:Computer design basics:

Datapath logic, arithmetic-logic unit, datapath representation, control logic, control word, simple computer architecture, instruction formats, instruction decoder, basic operation cycle, operand addressing, addressing modes, instruction set architectures,.

Text Books:

1. Morris Mano, Charles R. Kime, Tom Martin, “Logic and Computer Design Fundamentals”, Pearson.
2. Stephen Brown &ZvonkVranesic, “Fundamentals of digital logic with VHDL design”, TMH.

Reference Books:

3. Charles H. Roth Jr, “Fundamentals of logic design”, Thomson Learning.
4. Donald G. Givone, “Digital principles and design”, TMH.
5. Thomas L. Floyd, Digital fundamentals”, Prentice Hall.

D. CAD for VLSI Design

Unit 1

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

Unit 2

DESIGN RULES Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction

Unit 3

Placement and partitioning - Circuit representation - Placement algorithms - partitioning FLOOR PLANNING Floor planning concepts - shape functions and floorplan sizing.

Unit 4

Routing, Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

Unit 5

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis. MODELING AND SYNTHESIS High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

Text Books:

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002

REFERENCES

2.S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.

E. MEMS and NEMS TECHNOLOGY

Unit I: Overview and Introduction

Introduction to Design of MEMS and NEMS, Overview and Applications, Synergetic Paradigms, MEMS and NEMS Architectures, Coupled Systems, High-Level Design Issues, Modeling levels- Analytical or Numerical, Commercialization of MEMS/NEMS.

Unit II: MEMS/NEMS Systems and Devices

Force and Pressure Sensors, Resonant Sensor , Accelerometers- types and applications, Vibratory Gyroscopes, microbridge gas sensor, Metal-Oxide Nanowires for Gas Sensors, Thermal sensors, Silicon Nanowire Solar Cells, ZnO Nanowire UV Photodetectors, ZnO Nanowire Nanogenerator , MEMS/NEMS energy harvester, Mass flow sensor, Radiation sensor, Electrostatic Actuators- Comb Drive Actuator, Parallel-Plate Actuator, Cantilever Beam Actuator, Thermal Actuators, Digital Micromirror Device (DMD), Piezo-Phototronic Effect based devices, RF MEMS/NEMS Switch, MEMS/NEMS resonators. Inkjet nozzles, Introduction to Bio-MEMS/NEMS applications: - DNA Application, Lab-on-Chip, endoscopic pill camera. Drug delivery systems. Nanorobotics.

Unit III: Mathematical Modeling and Simulation CAD

Modeling Strategies: Lumped Parameter Modeling, Formulation of Dynamic Equations, Linear System Dynamics, Nonlinear Dynamics, Distributed Parameter Modeling, Equivalent Circuit Modeling, Models based on Hamilton's Principle. Synergetic Computer-Aided Design of MEMS, Introduction to MEMS simulators: COMSOL Multiphysics, CoventorWare, ANSYS, Intellisuite.

Unit IV: Materials, Fabrication for MEMS/NEMS

Silicon: Silicon oxide, nitride, carbide, Gallium arsenide and other group Ill-V compound, Semiconductors, Metals, Metal Alloys, thin metal films, Polymers, Glass and Quartz substrates, diamond, piezoelectric and magnetic compounds, Fundamentals of Metal–oxide Nanowires: ZnO. Microfabrication and Micromachining of Microdevices, Bulk Micromachining, Surface Micromachining, High-Aspect-Ratio (LIGA and LIGA-Like) Technology, Photolithography, Etching, Sol-gel deposition, SFB-DRIE, SCREAM, Molecular Beam Epitaxy Growth of Nanowires, Metal-oxide Nanowires by Thermal Oxidation Reaction Technique.

Unit V: Packaging for MEMS/NEMS

Packaging: Types of packaging, Ceramic, Metal, Molded plastic, Hermetic packaging, Die-attach process, Interconnects.

Text Books:

1. "Principles of Microelectromechanical Systems" - Lee, Ki Bang, John Wiley & Sons, 2011.
2. "MEMS and NEMS: Systems, Devices, and Structures" - Sergey Edward Lyshevski, CRC Press, 2002.

Reference Books:

1. "An Introduction to Microelectromechanical Systems Engineering" – Nadim Maluf, Kirt Williams, 2nd edition, Artech House, 2004.
2. "Analysis and Design Principles of MEMS Devices" - Minhang Bao, Elsevier, 2005.
3. "Microsystem Design" - Stephen D. Senturia, Kluwer Academic Publishers, 2002.
4. "Energy Harvesting Technologies" – Shashank Priya, Daniel J. Inman, Springer, 2009.
5. "Nanowires - Recent Advances" - Xihong Peng, InTech, 2012.
6. "Nanowires" - Paola Prete, InTech, 2010.
7. "Piezotronics and Piezo-Phototronics" - Zhong Lin Wang, Springer, 2012.
8. "Nanowires and Nanobelts, Materials, Properties, and Devices, Volume 2: Nanowires and Nanobelts of Functional Materials" - Zhong Lin Wang, Springer, 2006.

Paper Code: MECE-205
Paper Name: Elective – II

A. **Biomedical Signal Processing**
B. **Low Power VLSI Design**
C. **Embedded System Design**
D. **RF Integrated Circuits**
E. **Digital Image Processing**

A. BIOMDICAL SIGNAL PROCESSING

UNIT-I

Biomedical signals: Introduction to Biomedical Signals - ECG, EEG, EMG, ENG etc. Event related potentials. Biomedical Signal Analysis- Computer Aided Diagnosis; overview of analog signal analysis: time – and frequency-domain representation of signal, Fourier series and Fourier transform, linear system, correlation, convolution and filtering; random signal – correlation and spectral representation.

UNIT-II

Event Detection– Detection of P, QRS and T waves in ECG- EEG rhythms- Correlation and coherence analysis of EEG channels- Detection of EEG spike and wave complexes- Homomorphic filtering. Analysis of event related potential – Morphological analysis of ECG waves- Envelope extraction and analysis- Analysis of activity: zero crossing rates.

UNIT-III

Digital filters: FIR and IIR filter, biomedical applications of digital filtering- removal power line interference from ECG data, reducing ECG artifact from EMG data. ECG Pre-processing, wave form recognition, morphological studies and rhythm analysis, automated diagnosis based on decision theory, ECG compression, Evoked potential estimation.

UNIT-IV

HRV and Arrhythmia analysis: Heart rate variability-definition; comparison of short-term and long term HRV analysis; Time domain and spectral domain parametrs of short term recording.

UNIT-V

Neurological Signal : The Brain and its potentials; The Electrophysiology origin of brain waves; the EEG Signal and its characteristics; EEG analysis; EEG: evoked responses, averaging techniques, pattern recognition of alpha, beta, theta and delta waves in EEG waves, sleep stages, epilepsy detection, EMG: wave pattern studies.

TEXT/REFERENCE BOOKS

1. Biomedical Engineering Handbook, Author: J.D. Bronzino, Publisher: CRC press.
2. Textbook of Medical Physiology; Author: A C Guyton; Publisher: Prism Books (PVT) Ltd.
3. Fundamentals of Anatomy and Physiology, Author: F.H.Martini, Publisher: Prentice Hall
4. Modern Biomedical Signal Processing – Principles and Techniques, Author: D C Reddy TMH, New Delhi,2005.
5. Biomedical Signal Processing, Author: M Akay, Academic press, California,1994.
6. Biomedical Signal Processing, Author: W J Tompkins, Prentice hall of India, New Delhi, 1999

B. LOW POWER VLSI DESIGN

Unit-1

DEVICE & TECHNOLOGY IMPACT ON LOW POWER Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

Unit-2

SIMULATION POWER ANALYSIS AND PROBABILISTIC POWER ANALYSIS SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation,

Unit-3

Architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation - Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. LOW POWER DESIGN Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre computation logic

Unit-4

LOW POWER ARCHITECTURE & SYSTEMS, LOW POWER CLOCK DISTRIBUTION Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Unit-5

Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew,chip and package co-design of clock network ALGORITHM AND ARCHITECTURAL LEVEL METHODOLOGIES Introduction, design flow, algorithmic level analysis and optimization, Architectural level estimation and synthesis.

Text Books:

1. Gary K. Yeap, Farid N. Najm, “Low power VLSI design and technology”, World Scientific Publishing Ltd., 1996.

REFERENCES:

2. DimitriosSoudris, Christian Piguet, Costas Goutis,” Designing CMOS circuits for low power”,Kluwer Academic Publishers,2002

3. Kaushik Roy and Sharat C. Prasad,"Low-Power CMOS VLSI Circuit Design" ,Wiley- Interscience, 2000.

4. Chandrakasan, R. Brodersen , “CMOS Low Power Digital Design”, Kluwer Academic Publications. 1995. 5. Rabaey, M. Pedram, “Low Power Design Methodologies”, Kluwer Academic Publications. 1996.

6. Christian Piguet, “Low-power CMOS circuits: technology, logic design and CAD tools”, CRC Press, Taylor & Francis Group, 2006.

C. Embedded System Design

Unit 1

Embedded Systems, Processor Embedded into a System, Embedded Hardware Units and Devices In a System, Embedded Software in a system, Examples of Embedded Systems, Embedded System-on-chip (SOC) and Use of VLSI Circuit Design Technology, Complex Systems Design and Processors, Design Process in Embedded System, Formulization of System Design, Design Process and Design Examples, Classification of Embedded Systems, Skills Required for an Embedded System Designer

Unit 2

IO Types and examples, Serial communication devices, Parallel Device ports, Sophisticated Interfacing Feature in Devices Ports, Wireless Devices, Timer and Counting Devices, Watch dog timer, Real time clock, Network Embedded Systems, Serial Bus Communication Protocols, parallel Bus Devices protocolParallel communication Network using ISA, PCI, PCI-X and advanced buses, Internet Enabled Systems- Network protocols, Wireless and mobile system protocol.

Unit 3

Programmed-I/O Busy-wait Approach without Interrupt Services Mechanism, ISR Concept, Interrupt Sources, Interrupt Servicing(Handling) Mechanism, Multiple Interrupts, Context and the Periods for Context Switching, Interrupt Latency and Deadline, Classification of Processor Interrupt Service Mechanism from Context-Saving Angle, Direct Memory Access, Device Driver Programming

Unit 4

Multiple process in an application, Multiple Threads in an application,Task and Task state, Task and Data, Clear-cut Distinction between Functions, ISRS and Tasks by their Characteristics, Concept of Semaphores, Shared Data, Inter process Communication, Signal Function, Semaphore Functions, Message Queue Functions, Mailbox Functions, Pipe Functions, Socket Functions, RPC Functions

Unit 5

Operating system service, Process management, Timer function, Event function, Memory management, Device , File and I/O subsystem management, Interrupt routine in RTOS environment and handling of interrupt Sources calls, Real Time Operating Systems, Basic Design Using an RTOS, RTOS Task Scheduling Models, Interrupt Latency and Response of the Tasks as Performance Metrics, OS Security Issues

Text Books:

1. Jonathan W Valvano, Introduction to Embedded Systems Paperback – August 17, 2016, CreateSpace Independent Publishing Platform; 1 edition

Reference Books:

2. Yifeng Zhu, Embedded Systems with ARM Cortex-M Microcontrollers in Assembly Language and C: Third EditionJul 1, 2017, E-Man Press LLC, Latest Ed.

D. RF Integrated Circuits

Unit 1
Introduction
RF systems – basic architectures, Transmission media and reflections, Maximum power transfer, Passive RLC Networks,: Parallel RLC tank, Q,: Series RLC networks, matching: Pi match, T match

Unit 1
Passive IC Components: Interconnects and skin effect: Resistors, capacitors: Inductors, Review of MOS, Device Physics: MOS device review

Unit 1
Distributed Systems: Transmission lines, reflection coefficient, The wave equation, examples, Lossy transmission lines, Smith charts – plotting gamma

Unit 1
High Frequency Amplifier Design, Bandwidth estimation using open-circuit time constants, Bandwidth estimation using short-circuit time constants, Risetime, delay and bandwidth, Zeros to enhance bandwidth, Shunt-series amplifiers, tuned amplifiers, Cascaded amplifiers

Unit 5
RF Power Amplifiers: Class A, AB, B, C amplifiers: Class D, E, F amplifiers: RF Power amplifier design examples

Text/References:
1. The Design of CMOS Radio-Frequency Integrated Circuits by Thomas H. Lee. Cambridge University Press, 2004.
2. RF Microelectronics by Behzad Razavi. Prentice Hall,1997.

3. David M. Pozar, "Microwave Engineering," 2nd Edition, John Wiley 1998

E: Digital Image Processing

Unit-I

Digital Image processing, Need of DIP, Pixel, sampling and digitization, Relationship among pixels: Neighborhood, connectivity, adjacency, Distance measures: Euclidean distance, city block, chess board .

Unit-II

Image transformation, Need of transformation, Fourier transforms, DCT, Walsh Transform, K L transform.

Unit-III

Arithmetic operations such as addition, substraction, multiplication and division, Logical operations for binary images, Perspective transformation,, Interpolation and decimation.Image enhancement: Spatial domain methods include point processing, histogram based techniques and mask operations and frequency domain operations.

Unit-IV

Image restoration, Image registration, Image segmentation: discontinuity based approach (Point, line, and edge detection) and similarity based approach (Thresholding, region growing based, region splitting and merging), Color Image Processing.

Unit-V

Applications of DIP: Pattern recognition, texture classification, Face detection, Face recognition, Gesture recognition, Biomedical Image analysis.

Text Books:

1. Digital Image Processing by Rafael C Gonzalez and Richard Woods 3rd Edition, Pearson.

References Books:

2. Fundamental of Digital Image Processing by A.K .Jain, Pearson, 1st Edition.
3. Digital Image Processing by William K Pratt, John Wiley & Sons, 2nd Edition.

Paper Code: MECE-206
Paper Name: Advanced Analog VLSI Design Lab

Session- I:Design and simulation of other analog building blocks

a. Comparators
b. PLL
c. LDO
d. Bandgap

Session-II: ASIC Design Experiments (shall be carried out using Mentor Graphics/Cadence Tools)
1. Part-I: Backend Design Schematic Entry/ Simulation / Layout/ DRC/PEX/Post Layout Simulation of CMOS Inverter, NAND Gate, OR Gate, Flip Flops, Register Cell, Half Adder, Full Adder Circuits
2. Part-II: Semicustom Design HDL Design Entry/ Logic Simulation, RTL Logic Synthesis, Post Synthesis Timing Simulation, Place & Route, Design for Testability, Static Timing Analysis, Power Analysis of Medium Scale Combinational, Sequential Circuits
3. Part-III: High Speed/Low Power CMOS Design Designing combinational/sequential CMOS circuits for High Speed Designing combinational/sequential CMOS circuits for Low Power

Session-II: Introduction to advanced layouts
a. Layout of a band gap : resistance matching. BJT matching. Half-cell dummy BJT addition. Box-shielding of critical nets. Current mirror matching and current mirror routing to improve PSRR.
b. Layout of an LDO: POWER-mos layout planning with guard-rings. Introduction to locally connected PMOS-es. Introduction to EM.
c. Layout of an ADC : introduction to fringe CAP layout. Introduction to differential routing. Layout of a switched-cap comparator by half cell matching.

Session –IV: Mini Project
Introduction to chip-level layout: a 10 bit 1MSPS industry standard SAR ADC with internal power supplies and bandgap.

a. ESD planning.
b. POWER planning.
c. Top level floorplan.
d. LVS with BBOX.
e. LVS/DRC with all actual and GDSII delivery.
f. ERC check.

Paper Code: MECE-207
Paper Name: Advanced Digital VLSI Design Lab

Session – I:

1. Memories and State Machines: Read Only Memory (ROM), Random Access Memory (RAM), Mealy State Machine, Moore State Machine, Arithmetic Multipliers using FSMs using VHDL/Verilog.

2. FPGA System Design: Demonstration of FPGA and CPLD Boards, Demonstration of Digital design using FPGAs and CPLDs. Implementation of UART/Mini Processors on FPGA/CPLD etc.

Session –II :

1. ALU design and verification (8 bit).
2. Design and verification of a sequence detector system using state machine.

Paper Code: MECE-208
Paper Name: Grand Viva II

Based on semester subjects